REMARKS

Reconsideration of the present application is respectfully requested.

Applicant submitted formal drawings concurrently with the present application. However, neither the office action summary (PTO FORM-326) nor the office action itself indicates that the formal drawings were reviewed. Explicit acknowledgement and approval of the formal drawings is respectfully requested.

Applicant requests that the Examiner initial a copy of the form PTO-1449 accompanying the enclosed Request For Return of Initialed Form PTO-1449, as listed reference serial number 09/120,830 was mentioned on pgs. 1 – 2 of the specification (JP-A-11-97413 corresponds to serial number 09/120,830), but not initialed by the Examiner on the form PTO-1449 filed along with a corresponding IDS concurrently with the present application.

In accordance with the election of July 15, 2002, claims 1 – 5 and 9 have been canceled without prejudice. However, Applicant reserves the right to file a divisional application based upon these canceled claims.

Claims 6 – 8 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,525,549 to Fukada et al. (hereafter "Fukada"). For the reasons discussed below, claims 6 – 8, as amended, are now in condition for allowance.

Claim 6 has been amended to recite the novel embodiment disclosed on, for example, pgs. 5 – 6 in which a semiconductor sensor chip includes a front portion (N^- type epitaxial layer) 3 and a rear portion (P^- type silicon substrate) 2. The front and rear portion form a PN junction plane that is parallel to a front surface of the front portion 3 and a rear surface of the rear portion 2. A sensing element (strain gauges 6) is disposed in the front portion 3 in a vicinity of the front surface of the substrate. A diaphragm 2a is disposed on a rear surface of the rear portion 2 and

within a cavity 2c. A diffused layer 4a is disposed on and along the PN junction plane. The diffused layer 4a has a conductivity similar to the rear portion 2 but with a higher impurity density (P^+ type).

Fukada discloses a semiconductor acceleration sensor formed from a P type substrate 45 and an N type expitaxial layer 47 with an N^+ diffusion layer 46 therebetween. A second N^+ diffusion layer 49 is formed in a scribe line area. This second diffusion layer 49 is used as an electrode while the substrate 45 is electrochemically etched to form grooves 51. The first diffusion layer 46 helps a current to sufficiently flow from the second diffusion layer 49 to the parts to be etched. However, Fukada fails to disclose that the conductivity of either of these diffused layers (which is N^+ type conductivity) is similar to the conductivity of the rear portion (substrate 45 which has P type conductivity).

Therefore, because Fukada fails to disclose a diffused layer having a conductivity similar to that of the substrate, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. 102(b) be withdrawn.

Regarding the rejection of claim 7 under 102(b), claim 7 recites the novel embodiment disclosed, for example, on pg. 5, lines 25 – 26 in which the upper corners 2b of the cavities 2c are rounded from isotropic electrochemical etching. This rounding is further shown in, for example, FIG. 1.

Fukada shows in, for example, FIGS. 31 and 33 a semiconductor device that has cavities 51 with sharp rather than rounded corners. The corners of the cavities 51 in Fukada are similar to the upper corners 2b of the cavities 2c in the present invention prior to the isotropic electrochemical etching (shown in FIG. 2C of the present application).

The Examiner has alleged that because Fukada discloses that its substrate 45 is electrochemically etched it must also disclose rounded corners. Applicant respectfully traverses this allegation. The various figures of Fukada clearly show that the upper corners are sharp rather than rounded. Further, the Examiner cannot assume that the electrochemical etching of Fukada will result in rounded corners as in the present invention. As mentioned above regarding the rejection of claim 6 and below regarding the 103(a) rejection, the etching process of Fukada is different then the present invention because of the conductivity of the diffusion layers with respect to the substrate.

Therefore, because Fukada fails to disclose a semiconductor device that has cavities 51 with rounded corners, it is respectfully requested that the rejection of claim 7 under 35 U.S.C. 102(b) be withdrawn.

Regarding the rejection of claim 8 under 102(b), claim 8 depends from amended claim 6. Therefore, the rejection of claim 8 under 35 U.S.C. 102(b) should be withdrawn for the above-mentioned reasons with respect to amended claim 6.

Claims 6 – 8 have been alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Fukada. For the reasons discussed below, these claims, as amended, are now in condition for allowance.

The Examiner has alleged that it would have been obvious to one of ordinary skill in the art to have doped the diffusion layer of Fukada to have more impurities than the substrate as in the present invention. However, this allegation has been rendered *moot* due to the amendment of claim 6. Claim 6 now recites a diffusion layer diffusion layer with a conductivity type similar to a rear portion (substrate).

Further, Fukada teaches away from having a diffusion layer with a conductivity type similar to the rear portion. A *prima facie* case of obviousness may be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. (See MPEP 2144.05 III, Aug. 2001). Fukada discloses that the first diffusion layer 46 is for helping current to sufficiently flow from the second diffusion layer 49 to the parts to be etched. Namely, the first diffusion layer 46 reduces horizontal resistance of the epitaxial layer 47, thereby helping the current to flow to the area of the substrate 45 to be etched. (See Col. 11, Lines 10 – 15). However, if the first diffusion layer 46 (or the other diffusion layer 49) were modified to have a conductivity type similar to the substrate 45 (P-type) as in the present invention, the horizontal resistance of the epitaxial layer 47 (which is N-type) would be increased. This is clearly contrary to the teaching of Fukada.

Therefore, because Fukada teaches away from a diffusion layer having a conductivity type similar to a rear portion, it is respectfully requested that the rejection of claim 6, as amended, under 35 U.S.C. 103(a) be withdrawn.

Claims 7 – 8 depend from amended claim 6. Therefore, the rejection of claims 7 – 8 should be withdrawn for the above-mentioned reasons with respect to amended claim 6.

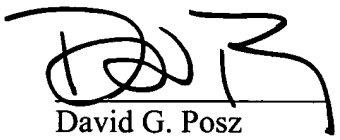
New claims 10 – 11 are presented for examination. These claims recite features that further distinguish the present invention from the art of record. Support for claim 10 can be found, for example, in FIG. 1. Support for new claim 11 can be found, for example, on page 9, lines 15 – 17.

In addition, new claims 10 – 11 depend from amended claim 1. Therefore, these claims should be allowed for the above-mentioned reasons with respect to amended claim 1.

Although no fees are believed to be due, permission is given to charge any unanticipated fees to Deposit Account 50-1147.

In view of the above amendments, additions and remarks, the present application is now believed to be in condition for allowance. Therefore, a prompt notice to that effect is respectfully requested.

Respectfully submitted,



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MARKED UP VERSION OF THE AMENDMENT SHOWING CHANGES MADE

IN THE CLAIMS

Claim 6 has been amended as follows:

6. (Amended) A semiconductor sensor chip comprising:

a semiconductor substrate having a front portion and a rear portion, the front portion and the rear portion having a different conductivity to form a P-N junction plane parallel to front and rear surfaces of the semiconductor substrate;

a sensing [elements formed on] element disposed in the front portion at a vicinity of the front surface of the semiconductor substrate;

a diaphragm [formed by making] contoured by a cavity extending from [on] the rear surface into the rear portion of the semiconductor substrate; and

a diffused layer [formed] disposed on and along the P-N junction plane and exposed to a side [surfaces] surface of the semiconductor sensor chip, the diffused layer having a same conductivity type as the rear portion where the cavity is located and having an impurity density higher than an impurity density of the rear portion [that] of the semiconductor substrate.